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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,834	06/20/2001	John F. Lane	10821/51085	4115

29934 7590 04/09/2007

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EXAMINER	
CORRIELUS, JEAN M	
ART UNIT	PAPER NUMBER
2162	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/885,834	LANE ET AL.	
	Examiner	Art Unit	
	Jean M. Corrielus	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on January 16, 2007, in which claims 1-4 and 10-13 are presented for further examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim1-4 and 10-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the claimed feature in claim 1 ***"a library of format writers, linked to the memory resident data model, for extracting and exporting into an export data file the at least one intelligent design stored in the memory resident data model"*** is not described in the specification to enable one having ordinary skill in the art to make and use the invention. The specification paragraph [0072] defines the use of exporting and importing of design and [0006] states that once captured, analyzed and resolved within the CAD/CAE system, design data is

then communicated throughout the rest of the company by extracting particular sections of the design in the form of partial ASCII files, hard copy plots or reports. However, such abovementioned of the specification does not extract nor export into an export data file at least one intelligent design. Based on the analysis provided above and substantial evidence or reasoning, the examiner provided that one having ordinary skilled in the art would not recognize in the disclosure a description of the invention defined by the claims. The limitation as claimed in claim 1 ***"a library of format writers, linked to the memory resident data model, for extracting and exporting into an export data file the at least one intelligent design stored in the memory resident data model" is*** not supported by the as-filed disclosure, which is violated the written description requirement. In re Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981). Applicant should duly note that the first paragraph of 35 U.S.C. 112 requires that the "specification shall contain a written description of the invention". Applicant should also note that the essential goal of the description of the invention requirement is to clearly convey the information that an applicant has invented the subject matter which is claimed; and to put the public in possession of what the applicant claims as the invention." Furthermore, the written description requirement of the Patent Act promotes the progress of the useful arts by ensuring that patentees adequately describe their inventions in their patent specifications in exchange for the right to exclude others from practicing the invention for the duration of the patent's term. Indeed, the specification doe not satisfy the written description requirement because the specification does not describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-4 and 10-13 as best understood by the examiner are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al., (hereinafter "Van") US Patent no. 5,920,873 and Southgate US Patent no. 6,161,211.

As to claims 1, 14 and 22, Van disclose a design control system usable in a concurrent engineering process to enable the design to be processed. In particular Van discloses the claimed "a library of format readers for reading at least one intelligent design saved in a specific format" by creating a model interactively with user activities (col.12, lines 65-66; col.100, lines 45-57); "a format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format" automatically creating a data structure type for each data design (col.15, lines 10-22; col.19, lines 5-24; col.20, lines 17-18); "an import application-programming interface linked to the format verifier for importing the intelligent design in the applicable format for viewing the intelligent design"importing a located filed by use of an application program interface with a collection of model management utilities (col.7, lines 24-28; col.12, line 66-col.13, line 11); "a memory resident data model, linked to the import application-provamming interface, is a database for storing the properties and functional characteristics of the intelligent design" (col.13, lines 12-16); "a query application-programming interface, linked to the memory resident data model, for searching for at least one element in the

memory resident data model" by receiving a request from the displayed client screen to fulfills the request by a providing a result which provides a dynamic way to track a model during the design phase (col.12, lines 55-66); and "a user interface, linked to the query application-programming interface, for interactively accessing the memory resident data model" as an application program interface that provides a control panel input, which allows creation of a model by interactive user activity and by importing file listings an(col.7, lines 22-28). However, Van does not explicitly disclose an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application. On the other hand, Southgate discloses an analogous system that is directed to software tools for facilitating automated circuit design (col.2, lines 33-38). In particular, Southgate discloses the claimed "an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application" and "library of format writers, linked to the memory resident data model, for extracting and exporting into an export data file the at least one intelligent design stored in the memory resident data model" (col.3, lines 23-67; col.4, lines 15-20; col.6, lines 12-24; col.8, lines 32-48; col.9, lines 1-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the design control system library provided therein (see Van.fig.5) would incorporate the use of an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention in a single software application, in same conventional manner as disclosed by

Southgate. One having ordinary skill in the art would have found it motivated to use such an automated format verifier of South gate into Van'system because the optimation and mapping processes of Van's system would make better decision, thereby improving the performance and efficiency of optimized routed netlist.

As to claims 3, Van discloses the claimed "at least one format writer, linked to the query application- programming interface, for controlling a local configuration and behavior of the user interface" (col.7, lines 22-30; col.15, lines 10-28).

As to claims 4, Heile discloses the claimed "a collaborative network element, linked by at least one medium to the memory resident data model, for using the apparatus across a global computer network" (col.3, lines 1-8; col.8, lines 20-24, lines 55-66).

As to claims 10, Heile discloses the claimed "wherein the memory resident data model stores a plurality of intelligent designs" (col.8, lines 30-34).

As to claims 11, Heile discloses the claimed "wherein the plurality of intelligent designs have different application formats" (col.6, lines 25-36).

As to claims 12, Heile discloses the claimed "wherein the memory resident data model stores the plurality of intelligent designs in a format that allows simultaneous viewing" (col.5, lines 25-53; col.6, lines 22-55; col.7, lines 23-32; col.17, lines 6-17; lines 30-40).

As to claims 13, Heile discloses the claimed "wherein the memory resident data model provides connectivity between analogous device elements in the plurality of intelligent designs" (col.7, lines 23-33).

7. Claims 1, 3-4 and 10-13 As best understood by the examiner are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al., (hereinafter "Van") US Patent no. 5,920,873 and Dole US Patent no. 6,634,008.

As to claims 1, 14 and 22, Van disclose a design control system usable in a concurrent engineering process to enable the design to be processed. In particular Van discloses the claimed "a library of format readers for reading at least one intelligent design saved in a specific format" by creating a model interactively with user activities (col.12, lines 65-66; col.100, lines 45-57); "a format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format" automatically creating a data structure type for each data design (col.15, lines 10-22; col.19, lines 5-24; col.20, lines 17-18); "an import application-programming interface linked to the format verifier for importing the intelligent design in the applicable format for viewing the intelligent design"importing a located filed by use of an application program interface with a collection of model management utilities (col.7, lines 24-28; col.12, line 66-col.13, line 11); "a memory resident data model, linked to the import application-provamming interface, is a database for storing the properties and functional characteristics of the intelligent design" (col.13, lines 12-16); "a query application-programming interface, linked to the memory resident data model, for searching for at least one element in the

memory resident data model" by receiving a request from the displayed client screen to fulfills the request by a providing a result which provides a dynamic way to track a model during the design phase (col.12, lines 55-66); and "a user interface, linked to the query application-programming interface, for interactively accessing the memory resident data model" as an application program interface that provides a control panel input, which allows creation of a model by interactive user activity and by importing file listings an(col.7, lines 22-28). However, Van does not explicitly disclose an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application. On the other hand, Dole discloses an analogous system that is directed to an integrated design environment for the designe and test of integrated circuits. In particular, Dole discloses the claimed "an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application" and "library of format writers, linked to the memory resident data model, for extracting and exporting into an export data file the at least one intelligent design stored in the memory resident data model" (col.6, lines 53-67; col.8, lines 34-44; col.9, lines 60-67; col.12, lines 58-67; col.14, lines 18-24; col.16, lines 58-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the design control system library provided therein (see Van.fig.5) would incorporate the use of an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention in a single software application, in same conventional

manner as disclosed by Dole. One having ordinary skill in the art would have found it motivated to use such an automated format verifier of Dole into Van'system because the optimation and mapping processes of Van's system would make better decision, thereby improving the performance and efficiency of optimized routed netlist.

As to claims 3, Van discloses the claimed "at least one format writer, linked to the query application- programming interface, for controlling a local configuration and behavior of the user interface" (col.7, lines 22-30; col.15, lines 10-28).

As to claims 4, Heile discloses the claimed "a collaborative network element, linked by at least one medium to the memory resident data model, for using the apparatus across a global computer network" (col.3, lines 1-8; col.8, lines 20-24, lines 55-66).

As to claims 10, Heile discloses the claimed "wherein the memory resident data model stores a plurality of intelligent designs" (col.8, lines 30-34).

As to claims 11, Heile discloses the claimed "wherein the plurality of intelligent designs have different application formats" (col.6, lines 25-36).

As to claims 12, Heile discloses the claimed "wherein the memory resident data model stores the plurality of intelligent designs in a format that allows simultaneous viewing" (col.5, lines 25-53; col.6, lines 22-55; col.7, lines 23-32; col.17, lines 6-17; lines 30-40).

As to claims 13, Heile discloses the claimed "wherein the memory resident data model provides connectivity between analogous device elements in the plurality of intelligent designs" (col.7, lines 23-33).

Remark

8. Applicant asserted that Van Huben and Southgate does not nor disclose or suggest a single application. The examiner has carefully considered the subject matter As argued, the rejections advanced by the examiner, and the evidence of obviousness relied upon by examiner as support for the rejections. In rejecting the claims under 35 U.S.C. 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. The examiner's position (see paragraphs 6 and 7) with respect to the assertion above is that Van Huben and Southgate does not disclose a single application comprising an automated format verifier. Huben, however, discloses a design methodology is provided by which the design of a circuit implemented from the top down, i.e., from the system requirements to the circuit level implementation, wherein the design methodology provides an approach to the design process in which design elements from different design levels are integrated into a design

hierarchy using a combination of new and currently available automated design tools. Such software allows the designer to make changes in any level of the design hierarchy which are automatically incorporated into other levels and provides some uniformity of design methodology and data formats so that design collaborators, which easily share information. Ultimately, by reducing the time between an idea and an operating circuit, wherein the designer employs a graphic editor to create a block diagram of the top level of his design as dictated by the relevant system requirements, and wherein for each of the blocks in the top level design, design file templates in any of a variety of formats are created in which the individual blocks are then implemented. . More specifically, Van Huben's system is related to methods useful in connection with the design development and manufacturing of complex electronic machine, wherein such concurrent engineering is enhanced and after creation of a model. Thereafter, the system of Van Huben provides continuously tracking the created model while allowing a user modification and allowing promotion of a model in the data processing system through the libraries. Such system of Huben has a functional limitation for receiving a request of a user by providing a dynamic way to track a model. From review of Huben's reference, the examiner has provided prima facie evidence that Huben is directed to the same field endeavor as Appellant's claimed invention. Therefore, Huben is an analogous art with respect to the invention as claimed.

On the other hand, discloses a design control system suitable for use in connection with the design of integrated circuits and other elements of manufacture having many parts which need to be developed in a concurrent engineering environment with inputs provided by users and or systems which may be located anywhere in the world providing a set of control information for coordinating movement of the design information through development

Thus, for the above reasons, it is believed that the rejection under 35 U.S.C. 103 provides substantial evidence to support the rationale statement in the above rejection, and the rejection under 35 U.S.C. 103 should be sustained.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean M. Corrielus whose telephone number is (571) 272-4032. The examiner can normally be reached on 10 hours shift.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean M Corrielus
Primary Examiner
Art Unit 2162

April 2, 2007